

**DYNAMIC RANDOM ACCESS MEMORY CELL AND METHOD FOR
FABRICATING THE SAME**

5 **CROSS-REFERENCE TO RELATED APPLICATION**

 This application claims the priority benefit of Taiwan application serial no. 92131757, filed on November 13, 2003, the full disclosure of which is incorporated herein by reference.

10 **BACKGROUND OF THE INVENTION**

Field of the Invention

[0001] This invention generally relates to a method for fabricating a semiconductor device, and more particularly to a dynamic random access memory (DRAM) cell and a method fabricating the same.

15 Description of Related Art

[0002] Capacitor plays an important role in storing data in a memory cell. The more charges the capacitor stores, lesser the noise will affect the reading/writing process for a memory cell. There are several ways to increase the capacitance such as increasing the surface area of the capacitor. However, this also increases the size of the memory device. How to increase the capacitance without increasing the size of the memory device is an important issue, especially when the integration level is getting higher and higher.

[0003] A conventional deep trench capacitor has been widely used in memory devices as shown in FIG. 1. FIG. 1 is a cross-sectional view of a DRAM cell with a

deep trench capacitor.

[0004] Referring to FIG. 1, the conventional DRAM cell includes a deep trench capacitor 140 and a transistor 150. The deep trench capacitor 140 is configured inside the substrate 100. The deep trench capacitor 140 includes polysilicon layers 106a, 106b, and 106c in the deep trench 110 as the upper electrode, an buried electrode region 102 as the bottom electrode at the periphery of the deep trench 110, and a capacitor dielectric layer 104 between the upper and bottom electrodes. The deep trench capacitor 140 uses the polysilicon layers 106a, 106b, and 106c as the upper electrode. Further, the buried electrode regions 102 and 112 are implanted inside the substrate 100. To form this structure, the manufacturing process is very complex. Further, the conventional DRAM cell includes the transistor 150. The transistor 150 includes a gate electrode 130 above the substrate 100 and the drain/source regions 132 in the substrate 100 beside the two sides of the gate electrode 130. A collar oxide layer 108 is also disposed between the polysilicon layer 106b and the substrate 100 to isolate the polysilicon layer 106b and the buried electrode region 112. A buried strap 114 is further disposed in the substrate 100 adjacent to the polysilicon layer 106c. Hence, how to simplify the structure and the manufacturing process of the DRAM cell is an important issue. Further, since the deep trench capacitor is deep, a capacitor with a larger cross section is required to facilitate the filling of the polysilicon layers. Ultimately, the size of the conventional deep trench capacitor cannot be reduced with the increase of the integration level.

SUMMARY OF THE INVENTION

[0005] An object of the present invention is to provide a DRAM cell and a

method for fabricating the same to reduce the size of the DRAM cell.

[0006] Another object of the present invention is to provide a DRAM cell and a method for fabricating the same to simplify the manufacturing process and to reduce the costs.

5 [0007] Still another object of the present invention is to provide a DRAM cell and a method for fabricating the same to obtain a higher capacitance coupling rate.

[0008] Further still another object of the present invention is to provide a DRAM cell and a method for fabricating the same to be compatible with the logic process and be used in system-on-chip (SOC).

10 [0009] The present invention provides a method for fabricating a trench capacitor. The method includes: forming a trench in a substrate; forming a first capacitor dielectric layer on the surface of the trench; forming a conducting layer inside the trench; forming a second capacitor dielectric layer on the surface of the substrate and on the conducting layer, the substrate encompassing the periphery of the first and
15 second capacitor dielectric layers being a bottom electrode; forming a protruding electrode on the substrate, the protruding electrode being on the substrate around the trench and covering a junction between the trench and the substrate; and electrically connecting the protruding electrode and the conducting layer, the conducting layer and the protruding electrode being an upper electrode.

20 [0010] The present invention provides a method for fabricating a DRAM cell, comprising: forming a trench in a substrate; forming a first capacitor dielectric layer on the surface of the trench; forming a conducting layer inside the trench; forming a second capacitor dielectric layer on the surface of the substrate and on the conducting layer, wherein the substrate encompassing the periphery of the first and second capacitor

dielectric layers serves as a bottom electrode; forming a protruding electrode and a gate electrode on the substrate, the protruding electrode being on the substrate around the trench and covering a junction between the trench and the substrate; forming a plurality of drain/source regions inside the substrate, the plurality of drain/source regions being
5 beside two sides of the gate electrode; and electrically connecting the protruding electrode and the conducting layer, the conducting layer and the protruding electrode being an upper electrode.

[0011] The present invention provides a trench capacitor, comprising: a substrate having a trench; a conducting layer filling the trench and extending to the
10 substrate around the trench; and a capacitor dielectric layer between the surface of the trench and the conducting layer and between the conducting layer and the substrate, the conducting layer being an upper electrode, while the substrate encompassing the capacitor dielectric layer being a bottom electrode.

[0012] The present invention provides a trench capacitor, comprising: a
15 substrate having a trench; a conducting layer filling the trench; a first capacitor dielectric layer between the surface of the trench and the conducting layer; a protruding electrode on the substrate around the trench and covering a junction of the trench and the substrate; a second capacitor dielectric layer between the conducting layer and the substrate, the substrate encompassing the first and second capacitor dielectric layers
20 being a bottom electrode; and a conducting structure electrically connecting the protruding electrode and the conducting layer, wherein the conducting layer, the protruding electrode, and the conducting structure serve as an upper electrode.

[0013] The present invention provides a DRAM cell, comprising: a substrate having a trench; a conducting layer filling the trench and extending to the substrate

around the trench; a capacitor dielectric layer between the surface of the trench and the conducting layer and between the conducting layer and the substrate, the conducting layer being an upper electrode, while the substrate around the capacitor dielectric layer being a bottom electrode; a gate electrode on the substrate beside the conducting layer; a plurality of drain/source regions in the substrate beside two sides of the gate electrode; and a gate dielectric layer between the gate electrode and the substrate.

[0014] The present invention provides a DRAM cell, comprising: a substrate having a trench; a conducting layer filling the trench; a first capacitor dielectric layer between the surface of the trench and the conducting layer; a protruding electrode on the substrate around the trench, wherein the protruding electrode covers a junction of the trench and the substrate; a second capacitor dielectric layer between the conducting layer and the substrate, wherein the substrate around the first and second capacitor dielectric layers serves as a bottom electrode; a gate electrode on the substrate beside the protruding electrode; a plurality of drain/source regions in the substrate beside two sides of the gate electrode; a gate dielectric layer between the gate electrode and the substrate; and a conducting structure electrically connecting the protruding electrode and the conducting layer, wherein the conducting layer, the protruding electrode, and the conducting structure serve as an upper electrode.

[0015] The present invention provides a protruding electrode to cover the junction between the trench and the substrate and to serve a portion of the upper electrode. Hence, not only current leakage at the junction between the trench capacitor and the substrate is prevented, a higher capacitance coupling rate is provided. Further, because the present invention is compatible with the current logic process, manufacturing costs can be reduced, and the process can be simplified. Further, the

present invention can be applied to the SOC. In addition, in accordance to the present invention, an electrode protruded from the trench, the capacitance is larger than the conventional capacitor.

[0016] The above is a brief description of some deficiencies in the prior art and
5 advantages of the present invention. Other features, advantages and embodiments of the invention will be apparent to those skilled in the art from the following description, accompanying drawings and appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

10 [0017] FIG. 1 is a cross-sectional view of a DRAM cell with a deep trench capacitor.

[0018] FIGs. 2A-2H are the cross-sectional views showing the steps of the fabrication process for a DRAM cell in accordance with a preferred embodiment of the present invention.

15

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0019] FIGs. 2A-2H are the cross-sectional views showing the steps of the fabrication process for a DRAM cell in accordance with a preferred embodiment of the present invention. The present invention can be applied to system-on-chip.

20 Referring to FIG. 2A, a substrate 200 such as a silicon substrate is provided. A pad oxide layer 201 is formed on the substrate 200. Then, a mask layer 203 is formed on the pad oxide layer 201. Using the mask layer 230 as a mask, a trench 210 is formed by etching the substrate 200.

[0020] Referring to FIG. 2B, a capacitor dielectric layer 202 is formed on the

substrate to cover the surface of the trench 210. The capacitor dielectric layer 202 can be a SiO₂/Si₃N₄/SiO₂ (ONO) stacked layer, or a Si₃N₄/SiO₂ (NO) stacked layer.

[0021] Referring to FIG. 2C, a first conducting layer 204 is formed in the trench 210. The material of the first conducting layer 204 is, for example, doped polysilicon.

5 To form the first conducting layer 204 includes filling the trench 210 with a conducting layer, followed by removing the conducting layer and the capacitor dielectric layer 202 outside the trench 210 by chemical mechanical polishing (CMP) process. The patterned mask layer 203 can be used as an etching stop layer.

[0022] Referring to FIG. 2D, a portion of the first conducting layer 204 is
10 removed by etching back such that its top aligns with the surface of the substrate 200. The pad oxide layer 201 and the patterned mask layer 203 are then removed. At the same time, a portion of the capacitor dielectric layer 202 is also removed.

[0023] Referring to FIG. 2F, a dielectric layer is formed on the surface of the substrate 200 and the first conducting layer 204. The dielectric layer on the substrate
15 200 around the trench 210 can serve as another capacitor dielectric layer 206a. The dielectric layer farther away from the trench 210 can be the gate dielectric layer 206b. The material of the capacitor dielectric layer 206a and the gate dielectric layer 206b can be the same or different. If they are different, the capacitor dielectric layer 206a and the gate dielectric layer 206b can be formed respectively. The capacitor dielectric
20 layer 206a and the gate dielectric layer 206b can be a SiO₂/Si₃N₄/SiO₂ (ONO) stacked layer or a Si₃N₄/SiO₂ (NO) stacked layer. Further, the gate dielectric layer 206b can be an oxide layer. In addition, before forming the gate dielectric layer 206b, a well implantation process can be performed to form a well in the substrate (not shown). Taking PMOS as an example, the well formed in the substrate can be an N well. Then,

a second conducting layer 208, such as, doped polysilicon is formed in the substrate 200.

[0024] Referring to FIG. 2G, the second conducting layer 208 is defined to form a protruding electrode 208a and a gate electrode 208b. The protruding electrode 208a is located on the substrate 200 around the trench 210 and covers the junction between the trench 210 and the substrate 200. Hence, the capacitor dielectric layer 202 is prevented from being damaged due to subsequent processes, and ultimately, a leakage from the junction between the top of the trench 210 and the surface of the substrate 200 can be avoided. Further, the protruding electrode 208a can increase the capacitance coupling rate. The gate electrode 208b is located on the substrate 200 beside the protruding electrode 208a. Then, the spacers 209, such as silicon nitride spacers, can be formed on the sidewalls of the gate electrode 208b and the protruding electrode 208a. Thereafter, a drain/source implantation process is performed to form the drain/source regions 211 beside the sides of the gate electrode. Taking a PMOS as an example, the drain/source regions 211 are P-type regions. Then, a salicide process can be performed to form a self-aligned silicide layer (not shown) on the exposed surfaces of the gate electrode 208b and the protruding electrode 208a.

[0025] Referring to FIG. 2H, the protruding electrode 208a is electrically connected to the first conducting layer 204. To achieve that, an ILD layer 212 is formed on the substrate 200 to cover the protruding electrode 208a, the gate electrode 208b, the shallow trench isolation structure 220, and the first conducting layer 204. Thereafter, a contact window opening 214 is formed in the ILD layer 212 to expose a portion of the protruding electrode 208a and the first conducting layer 204. A conducting structure 216, such as, Cu or W, is formed in the contact window opening

214. After completing the steps of forming a DRAM cell, a negative voltage is applied to the protruding electrode 208a so that the substrate 200 around the capacitor dielectric layers 202 and 206a will be reversed to have the same polarity as the drain/source regions 211. Hence, the substrate 200 around the capacitor dielectric layers 202 and 206a is deemed to be the bottom electrode of the capacitor. Correspondingly, the capacitor dielectric layers 202 and 206a are the dielectric layers of the capacitor, whereas the conducting structure 216, the first conducting layer 204, and the protruding electrode 208a are the upper electrode of the capacitor. Further, the contact window opening 214 and the conducting structure 216 can be concurrently formed with the bit line of the DRAM so that no additional photolithography process is required.

[0026] In brief, the present invention provides a protruding electrode to cover the junction of the trench and the substrate and to serve as a portion of the upper electrode. Hence, leakage at the junction between the trench capacitor and the substrate can be prevented, and a higher capacitance coupling rate can be provided.

Further, because the present invention is compatible with the current logic process, the manufacturing costs can be reduced and the process is simplified. Further, the present invention can be applied to the SOC. Since the capacitor of the present invention has a simpler structure than the conventional deep trench capacitor, the costs can be effectively reduced. In addition, in accordance of the present invention, an electrode is protruded from the trench, the capacitance is larger than the conventional capacitor. Hence, the capacitor of the present invention can provide the required capacitance and is suitable for the fabrication of a smaller device while maintaining the requisite capacitance.

[0027] The above description provides a full and complete description of the

preferred embodiments of the present invention. Various modifications, alternate construction, and equivalent may be made by those skilled in the art without changing the scope or spirit of the invention. Accordingly, the above description and illustrations should not be construed as limiting the scope of the invention which is

5 defined by the following claims.